AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A chip-stack semiconductor device, comprising:

multiple semiconductor chips vertically stacked on top of each other, wherein:

each of the semiconductor chips includes electrode pads, and

multiple through electrodes formed in a region within the electrode pads, wherein ~~at least two of the through electrodes formed in a region within the same electrode pad are not in direct electrical contact with each other~~ at least one type of the through electrodes is a non-contact through electrode that is not electrically connected to an electrode pad of the semiconductor chip in which the non-contact through electrode is formed.

2. (Previously presented) The chip-stack semiconductor device as set forth in claim 1, wherein for at least one semiconductor chip the electrode pads are provided along a periphery of the semiconductor chip so as to surround a device region.

3. (Original) The chip-stack semiconductor device as set forth in claim 1, wherein at least one type of the through electrodes is contact through electrodes electrically connected to the electrode pad.

4. (Original) The chip-stack semiconductor device as set forth in claim 2, wherein at least one type of the through electrodes is contact through electrodes electrically connected to the electrode pad.

5-6. (Canceled)

7. (Original) The chip-stack semiconductor device as set forth in claim 1, wherein a through electrode is further provided in regions outside of the electrode pad.

8. (Original) The chip-stack semiconductor device as set forth in claim 2, wherein a through electrode is further provided in regions outside of the electrode pad.

9. (Original) The chip-stack semiconductor device as set forth in claim 1, wherein the through electrodes in the semiconductor chips are connected to each other via bumps so that the semiconductor chips are vertically stacked on top of each other.

10. (Original) The chip-stack semiconductor device as set forth in claim 2, wherein the through electrodes in the semiconductor chips are connected to each other via bumps so that the semiconductor chips are vertically stacked on top of each other.

11-18. (Canceled)

19. (Previously presented) The chip-stack semiconductor device of claim 1, wherein the electrode pads are electrically connected with a device region of the semiconductor chip.

20. (Currently amended) A chip-stack semiconductor device, comprising:

multiple semiconductor chips vertically stacked on top of each other, and at least first and second electrode pads provided on at least one of the semiconductor chips wherein:

each of the semiconductor chips includes multiple through electrodes connected to each other in regions inside of electrode pads, each of the through electrodes linking a front surface to a back surface of the semiconductor chip; and

wherein a plurality of different through electrodes are provided in the first electrode pad, so that when viewed from above the plurality of through electrodes are located inside a periphery of the first electrode pad, wherein ~~at least two of the through electrodes formed in a region within the same electrode pad are not in direct electrical contact with each other~~ at least one type of the through electrodes is a non-contact through electrode that is not electrically connected to an electrode pad of the semiconductor chip in which the non-contact through electrode is formed.

21. (Previously presented) The device of claim 20, wherein of the plurality of different through electrodes provided in the first electrode pad, first and second of these different through electrodes carry different signals.

22. (Previously presented) The device of claim 20, wherein of the plurality of different through electrodes provided in the first electrode pad, first and second of these different through electrodes carry different signals and extend to different depths in the semiconductor device.

23. (New) A chip-stack semiconductor device, comprising:

multiple semiconductor chips vertically stacked on top of each other, wherein:

each of the semiconductor chips includes electrode pads, and

multiple through electrodes formed in a region within the electrode pads, wherein at least two of the through electrodes formed in a region within the same electrode pad are not in direct electrical contact with each other, and wherein the through electrodes are provided in respective apertures defined in the electrode pads so as to extend through the pads.